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LUT-BASED POWER MACRO-MODELLING TECHNIQUE FOR DIGITAL SYSTEMS

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Abstract: In this paper, a power macro-modelling technique at register transfer level (RTL) for the digital electronic systems composed of intellectual property (IP) components by using the statistical knowledge of their primary inputs/output is presented. During the power estimation procedure, the sequence of an input stream is generated by a genetic algorithm using input metrics. Then, a Monte Carlo zero delay simulation is performed and a power dissipation macro-model function is built from power dissipation results. From then on, this macro-model function can be used to estimate the power dissipation of the system just by using the statistics of the IPs primary inputs/outputs. In the correct work with the test IP system, the average error is 26%.

Keywords: Digital system, Power macro-modelling, LUT, RTL, power estimation, macro-blocks, Intellectual property, Genetic Algorithm

Introduction

In the VLSI (very large scale integration) chip design performance, area, reliability and cost have historically been the major considerations. In early VLSI design, the motivation was to find acceptable balance among these often conflicting considerations. But recently, low power consumption has become most important objective as a design constraint.

During the years of inception, the use of integrated circuits (IC) was confined to traditional digital electronic systems such as communication systems, and portable devices. Nowadays not only those devices play an increasingly important role but also the use of integrated systems is much more widespread, from controllers used in home appliances to the automobile industry. The digital electronic circuits are becoming more application specific. According to the Moore's law IC densities and operational frequencies will double every generation. The shrinking of devices due to developed fabrication technology has increased dramatically. The chip density is being used to extend the functionalities on a single Application Specification Integrated Circuit (ASIC) to the point where we can now get an entire System-on-Chip (SoC). More than 95% of current microprocessors are going into SoC designs. Therefore, the problems caused by power increases as the feature sizes decrease (shown in Table. 1 [1]).

However, the importance of low power dissipative digital circuits is being increased rapidly. For many consumers electronic applications low power dissipation is desirable. The battery lifetime may be the decisive factor in the success of the product. Consequently, it is widely said that microprocessor can no longer rely solely on device technology and circuit optimization to meet the power requirements. A key challenge in the low power systems is the accurate and fast power estimation. Power analysis at higher design level, such as computer architecture and software engineering, is called for providing new solutions to power problems [3], [4]. Hence, design and estimation techniques for low power

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Table 1 Forecast of ASIC power consumption [After Reference 1]

Year	2003	2004	2005	2006	2007	2010	2013	2016
Feature Size/nm	107	90	80	70	65	45	32	22
MTransistors/chip	910	1020	1286	1620	2041	4081	8163	16326
Max Clock/GHz	3.1	4.0	5.2	5.6	6.7	11.5	19.3	28.8
Main Voltage/V	1.1	1.1	1.0	1.0	0.9	0.8	0.7	0.6
Power (high)/W	150	160	170	180	190	218	251	288
Power (battery)/W	2.8	3.2	3.2	3.5	3.5	3.0	3.0	3.0

are keys to a successful SoC design.
There is another reason that high-level power analysis is demanded: the rapid growth of system design cost. As system becomes larger and more complex, circuit design and verifications become increasingly difficult and time consuming. Power and performance analysis at early stages of design flow is essential for shortening turn-around time. The design cost and time-to-market of electronic systems can be greatly reduced through the reuse of predesigned circuits. In this approach, components from possibly different intellectual property (IP) vendors are combined to form complete programmable systems. To support the exploration of the numerous architectural alternatives that can arise when designing IP components, and fast and accurate electronic design automation (EDA) tools are required to evaluate key design characteristics such as timing, area and power dissipation.

The use of silicon IP has been proposed as one possible solution to the problems associated with SoC design. The designers need to leverage on pre-validated components and IPs. Design methodology further supports IP reuse in a plug-and-play fashion, including buses and hierarchical interconnection infrastructure. Reuse design techniques employing IP cores cuts down on time-to-market and fast estimation shortens the design evaluation time, which is more efficiently used in design-space exploration. Estimation models for energy/power can be used based on design descriptions at various levels of abstraction such as gate, architecture level, with corresponding variations in speed and accuracy of estimation.

Power analysis of IP-based system is particularly a challenging task at the architecture level, because the designers need to compute accurate power estimates without direct knowledge of IP design details. Although it is possible for IP vendors to capture timing and area using a single number, the characterization of power in a simple manner has remained elusive, since the power dissipation depends on the actual input data [2], [5], which is unknown to the IP designers. On the other hand, with the wide deployment of mobile systems, low power chip design is becoming an increasingly important focus of VLSI research. Thus, at the architecture level the development of efficient and effective power estimator for IP-based systems is important and urgent to the VLSI design communities.

In response to this need, the power

macro-modeling technique is a promising solution to face the problem of high-level power estimation. The macro-model construction consists of generating a mapping between the power dissipation of a circuit and certain statistics of the input signals. This technique has been proven to be effective for individual IP components building IP power models [6]. The urgent need of a feasible IP power model is becoming more useful in recent years. The application of power macro-modeling on the IP blocks of an entire system requires knowledge of the signal statistics among the different IP blocks. To obtain this information, the architect must perform different functional simulations.

In this paper, we present a power estimation methodology at RTL based on macro- modelling techniques applied on IP-based systems. Various power estimation techniques have been introduced previously. They can be divided into two categories: probabilistic and statistical. Probabilistic techniques [7], [8], [9] use the probabilities of the input stream and their propagation into the circuit to estimate the internal switching activities of the circuit. These techniques are very efficient, but they cannot capture accurately factors like glitch generation, propagation, etc. On the other hand, in statistical techniques [10], [11], [12] the circuit is simulated under randomly generated input patterns and the power dissipation is monitored using a power estimator. Therefore, the power values obtained are used to estimate the power consumption for every input stream. For accurate power estimation, we need to produce a required number of simulated vectors, which is usually high and causes run time problem. To handle this problem, a Monte Carlo simulation technique was presented in [13] that use input vectors randomly generated to obtain the power values. Several samples combined with previous ones are required to determine whether the entire process needs to be repeated in order to satisfy a given criteria. Most existing approaches of statistical power estimation consider the input signal probabilities and their average switching activities of the input signal and use signal probabilities propagation methods to estimate the internal switching activities [14]. In those approaches, there is no guarantee that the estimated power keeps any relation with the real dissipation of the circuit. To solve this problem, a look-up table (LUT) based macro-model was presented in [15] and further improved in [16] that stores the equi-spaced discrete measured power values of the input signal statistics. The interpolation method was introduced in the case of the input statistics do not correspond to any value stored on the LUT. In [17], [18] the interpolation scheme was improved by using the power sensitivity concept. For better accuracy, numerous power macro-modelling techniques [19], [20] have been introduced.

In recent work [21], the authors used analytical macro-modelling approach without considering temporal correlation T_{in}. The temporal correlation captures those features that missed on spatial correlation S_{in}. In this paper, we continue our previous research in [29], [22], [23] developing power macro-modelling technique based on the power estimation methodology using temporal correlation. Our model is LUT based. The input metrics of our macro-model are the average input signal probability Pin, the average input transition density Din, the input spatial correlation Sin, and the input temporal correlation Tin. Our macro-modelling technique achieves relatively good accuracy. In our experiments, a test IP-based system is used including the IP macro-blocks.

The rest of this paper is organized as follows. In Section 2, we shortly discuss the problem formulation. In Section 3 we give the background for the input parameters of our power macro-model

and proposed power estimation methodology. This macro-model is evaluated in Section 4. Section 5 summarizes our work.

2. Problem Formulation

For the construction of power macro-model to the IP-based test system ***M***, the given statistical signals at different input nodes ***Q***, the algorithm generates an input signals according to metrics P_{in}, D_{in}, S_{in}, T_{in}. The output metrics P_{out}, D_{out}, S_{out}, T_{out} can be extracted by the functional simulations at the outputs of *M* as shown in Fig. 1. The power estimation problem for ***M***, under the zero-delay model can be stated as:

"Given the RTL description of a IP-based test system with ***N*** *inputs and* ***M*** *outputs and the zero-delays of its gates, and assuming that the period of the applied input vectors is greater or equal to the settling time of the circuit, estimate the average power consumption of the circuit for an input vector stream through the calculation of the circuit average switching activity."*

The accuracy of the switching activity evaluation is strongly depended on the data correlation of the circuit signals and the assumed zero gate delay model. Concerning data correlation, it includes the temporal and spatial correlation. By temporal correlation we mean the dependency of a signal on its previous values. The spatial correlation is divided to the structural correlation, which is coming from the reconvergent fanout nodes, input pattern dependency coming from the sequence of the applied input vectors. In case of zero delay model, a gate performs at most one transition in a clock cycle, which is called functional or useful transition. However, under real-delay model the gate may perform additional transitions called spurious transitions or glitches. In most practical circuits, except those circuits that are largely based on exclusive-or gates, the glitch power only accounts for an average of 20- 30% of the real-delay power [24].

3. Power Macro-modelling Methodology

One of the most challenging aspects in the construction of a power macro-model is the choice of the model's input parameters, or metrics. These metrics should be capturing the features that are primarily responsible for a system's dissipation and can thus help in obtaining good estimates of its power dissipation. We focus on the problem of statistical power macro-modelling at register transfer level for IP-based designs. Our model is LUT based. The input output (I/O) metrics of our macro-model are the average input signal probability P_{in}, average input transition density D_{in}, input spatial correlation S_{in}, input temporal correlation T_{in}, average output signal probability P_{out}, average output transition density D_{out}, output spatial correlation S_{out} and output temporal correlation T_{out}.

Once the I/O metrics are selected, the input sequences are computed by our genetic algorithm (GA) [25], [26] while output metrics are extracted from the functional simulations using simulator as shown in Fig. 2. This section describes and motivates the metrics of our macro-model.

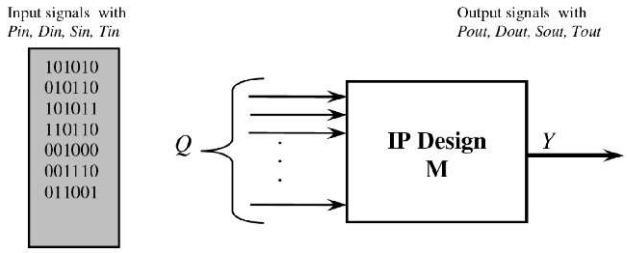

Fig. 1. Block diagram of IP design: All inputs have different input signals

3.1 Input Macro-modelling for IP-based Macro-blocks

Since the power is dependent on circuit inputs, it is clear that a power macro-model should take the input activity into account. When the circuit is modelled then a simple modelling strategy is to create a table that gives the power for every possible input vector pair. This leads to a trade-off between the amount of detail that one includes about the inputs and the accuracy resulting from the model. One possibility is to consider the average input signal probability P_{in}, average input transition density D_{in}, input spatial correlation S_{in}, and input temporal correlation T_{in} at every input node m_i and to build a model that depends only on these four variables. We have considered four-dimensional look-up-table. In this case, two different input assignments of P_{in}, D_{in}, S_{in}, T_{in} values, which may lead to different power values, may have same and the LUT would predict the same for both assignments, obviously with some error. Similar power macro-modelling techniques were presented in [21], [17]. Our macro- model consists of a nonlinear function based on LUT approach. This model estimates the average power dissipation P_{IP_avg} of IP macro-block using "(1)".

$$P_{IP\_avg} = f(P_{in}, D_{in}, S_{in}, T_{in}) \qquad (1)$$

The macro model function $f(.)$ in "(1)" is obtained by a given IP macro block which maps the space of input signal properties to the power dissipation of a circuit .When the input metrics of $f(.)$ are solely determined by the input signals the computation of power estimates is a straight forward and fast function evaluation . The most commonly used templates for the macro model function $f(.)$ are low order polynomial functions . For a *kth* order complete polynomial function with n input parameters ,a total of S^{k}_{n+k} coefficients need to be computed . The IP macro-blocks are simulated under different sample streams with, P_{in}, D_{in}, S_{in}, T_{in}. This model estimates the average power dissipation. Given an IP macro-block with the number of primary inputs r and the input binary stream

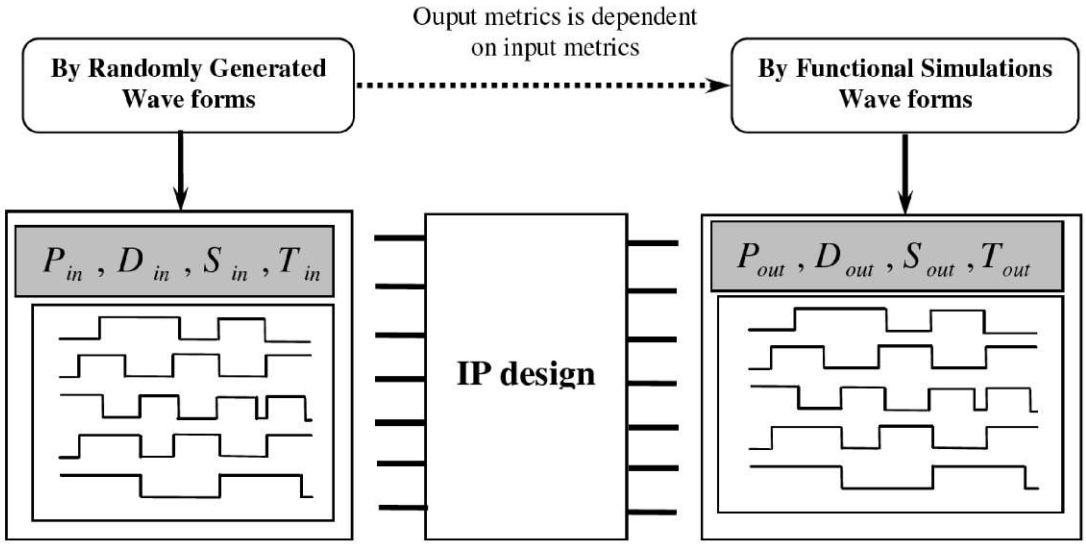

Fig. 2. Extraction of input/output metrics

q = {(q_{11},$q_{12}$$q_{1r}$), ($q_{21}$$q_{22}$,....,$q_{2r}$),..., ($q_{s1}$, q_{s2},..., q_{sr})} of length s, these metrics are defined as follows [15], [16], [27], [28] using "(2)", "(3)", "(4)" and "(5)".

$$P_{in} = \frac{\sum_{i=1}^{r} \sum_{j=1}^{s} q_{ij}}{r \times s} \quad (2)$$

$$D_{in} = \frac{\sum_{j=1}^{r} \sum_{i=1}^{s-1} q_{ij} \oplus q_{i+1\,j}}{r \times (s-1)} \quad (3)$$

$$S_{in} = \frac{\sum_{j=1}^{r} \sum_{k=1}^{r} \sum_{i=1}^{s} q_{ij} \oplus q_{ik}}{s \times r \times (r-1)} \quad (4)$$

$$T_{in} = \frac{\sum_{j=1}^{r} \sum_{t-1}^{s-t+1} (y_j \otimes q_j)}{r \times s} \quad (5)$$

In the estimation procedure, the actual signal statistics are derived and applied to f(.) in "(1)" to compute the power estimate. Power sensitivity of input metric **R** shows how **R** effects **P** and is defined in [20], [21]:

$$\lim_{\Delta R \to 0} \frac{\Delta P}{\Delta R} \quad (6)$$

Intuitively, the higher the sensitivity of **R** should be used in the characterization phase to increase the accuracy of power macro-modelling. Given an analytical expression f(.), the power sensitivity can be calculated by the partial derivation of f(.).

3.2 Output Macro-modelling for IP-based Macro-blocks

Output macro-modelling was first introduced in [28] to predict output signal statistics of an individual IP block from input signal statistics. In our output macro-modelling, we propose a new method to the computation of power macro-model f(.) in "(1)" can be used to a circuit to its output signal statistics. In the characterization step, functional simulation of the circuit is performed with different input sequences to obtain output metrics. The output metrics are the average output signal probability P_{out}, average output transition density D_{out}, output spatial correlation S_{out} and output temporal correlation T_{out}. The function f(.) in "(1)" can be used to construct to a set of functions f_A, f_B, f_C and f_D that maps the input metrics of a macro-block to its output metrics P_{out}, D_{out}, S_{out}, T_{out} are derived in "(7)", "(8)", "(9)", "(10)":

$$Pout \quad f_A(P_{in}, D_{in}, S_{in}, T_{in}) \quad (7)$$

$$Dout \quad f_B(P_{in}, D_{in}, S_{in}, T_{in}) \quad (8)$$

$$Sout \quad f_C(P_{in}, D_{in}, S_{in}, T_{in}) \quad (9)$$

$$Tout \quad f_D(P_{in}, D_{in}, S_{in}, T_{in}) \quad (10)$$

Similar to power sensitivity in "(6)", the sensitivity of an output metrics with respect to P_{in}, D_{in}, S_{in}, T_{in} is defined as the partial derivation of the corresponding function f_i.

3.3 Monte Carlo Simulation

The Monte Carlo approach for power estimation was first proposed by F. Najm [13]. The method estimates the average power by sampling the input vectors with certain length l from the original sequence and fed them into the simulator to derive a sample value of the average power. The average power consumption can be estimated with the average of several sample values. From the Central Limit Theorem, the sample values can be presumed as a Normal distribution when l approaches infinity. The probability that the estimated mean is within a certain error range of the real mean can be also derived under the assumption. If l is *far* from a Normal distribution, the basis of the Monte Carlo method fails and the estimated power may have a larger error level than expected.

We assume that a hierarchical netlist of the circuit with each IP module described at the RTL. For each module, a power dissipation technique at the same abstraction level as the netlist is adopted. Our target is the average total power consumption of a hierarchical circuit under a user-specified application input

stream. In addition, the estimation itself is performed in a single Monte Carlo simulation so that the power estimate at the top level circuit satisfies the user-specified confidence and error levels. This is different from the strategy which estimates each IP module in a separate Monte Carlo simulation and sums up the estimates to produce total average power. The drawback of the latter strategy is that it is difficult to determine a prior what confidence and error levels should be assigned to each module so that the sum of individual power estimates satisfies the confidence and error levels specified at the top circuit level. In our experiments, we performed Monte Carlo zero delay simulation technique for the digital IP-based system and the power dissipation is obtained by our macro-model function.

The interpolation scheme [20], [21] can be applied (to improve the power sensitivity concept), if the input metrics do not match on their characteristics. The block diagram in Fig.3 gives an overall view of the RTL power estimation technique. This technique uses an input model based on a Markov process to generate the input stream for simulation is discussed in [20], [25]. The simulation is performed in an iterative fashion. The vector sequence of fixed length (sample) is simulated during every iteration. The simulation results are monitored to calculate the mean value and variance of the samples. The iteration terminates when the some stopping criteria is met. At the end, the power values are observed when the successive numbers of iterations have done.

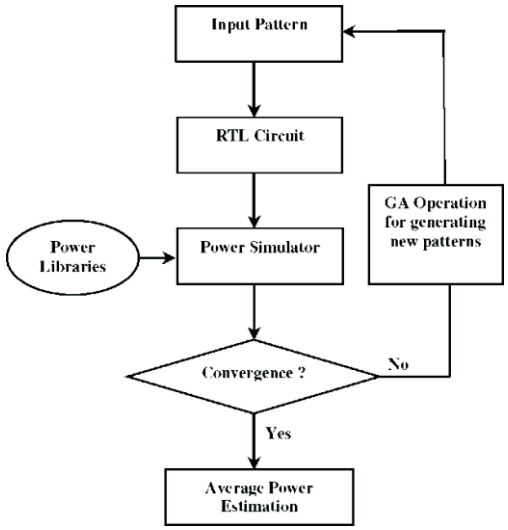

Fig. 3. The flow of RTL power estimation

3.4 Power Macro-Modelling for IP-based Digital System

Several approaches [18], [16], [20] have been proposed to construct power macro-models on ISCAS-85 benchmark circuits. We have observed that the same methodology works as well for different IP macro-blocks such as array multipliers, comparators, delay elements (shift registers), adders in terms of the statistical knowledge of their primary inputs/outputs. Recently we have presented in [29], [22], [23] a macro-model for different IP blocks. The proposed methodology was described as follows: in our static power macro-modeling procedure, the sequence of an input stream was generated for a desired input metrics: P_{in}, D_{in}, S_{in}, T_{in}. Then using functional simulations and a power estimator, the output stream sequence and the average power dissipation P_{lP_avg} was extracted by the output waveforms of the IP macro-block. At this moment, the power function in "(1)" can be defined. All this process is divided in two steps. In the first one, the metrics of the inputs/outputs (I/O) sequences were computed by our GA [25], [26] and the power function was obtained using P_{lP_avg} in (1). The interpolation scheme [17], [18] can be applied (to improve power sensitivity concept), if the input metrics

do not match based on their characteristics. In the second one, Monte Carlo zero delay simulation [8] was performed with different sequences of their signal statistics to evaluated the quality of the power function P_{lP_avg} . At the end we get the power results.

In this section, we continue our previous work and present the application of the statistical power estimation method for IP-based system. In our preliminary work, the approach intends to reduce the intensive amount of simulations at a higher abstraction level. We use the same IP blocks presented in [29], [22], [23] and their macro-model information for our IP-based system. Now, instead of simulating every IP block, we applied the Monte Carlo zero delay simulation to the entire test IP-based system. These macro-blocks are connected together to construct the test IP system as shown in Fig. 4.

The application of the power macro - modeling on each IP block requires knowledge of the input signal statistics among these blocks . To obtain this information , different functional simulations need to be performed with different input statistical values of each IP macro block .For example in Fig .4 , the inputs of the block IP A1 are the inputs of the test IP system ,while the outputs of IP A1 are the inputs of IP A2 and IP S1 IP block can be used as input signal statistics of the reference and so on . The output signal statistical information for each IP block can be used as input signal statistics of the reference connected IP macro block . For IP A1 block ,we generate random input vectors of 25 different values using input metrics P_{in}, D_{in}, S_{in}, T_{in}. Then to construct the LUT , the test IP system is simulated 25 times and for each IP block ,25 different values of input metrics are measured using functional simulations . The average power dissipation *Psystem* is extracted using "1( ) " .

$$P_{system} = \sum_{i=1}^{n} P_{IPi\_avg} \qquad (11)$$

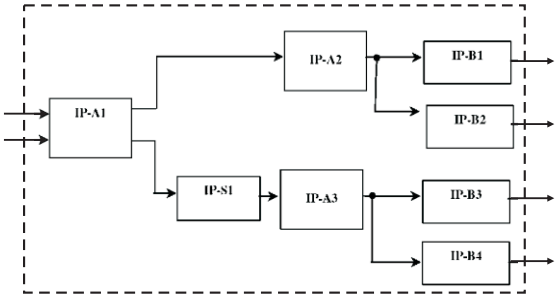

Fig .4. Test IP based system

We compare the estimated power P_{system} in "(11)" with the simulated power estimation to evaluate the accuracy of the power macro-model function in "(1)". The reference values of the circuit's power dissipation are obtained using time delays from the Synopsys Power Compiler.

4. Experimental Results

In this section, we show the results of LUT based power macro-modeling approach. This approach has been implement to build the power macro-model at the RTL. The accuracy of the proposed model is evaluated for our test IP-based system. To do this, we generate random input vectors for different values of P_{in}, D_{in}, S_{in}, T_{in}. The input chosen sequences are highly correlated and they are generated by our new method. The power is estimated using Monte Carlo zero delay simulation technique. The power values extracted by LUT are compared to those obtained from simulations, and the average error is computed. The experimental results show that the randomly generated sequences have relatively accurate statistics and highly convergence. For the input metrics, P_{in}, D_{in}, S_{in}, T_{in} the value range is between [0, 1]. Several sequences with 8, 16, 32 bits wide are generated. The sequence length is 2000 vectors for the entire test system.

In Table 2, we illustrate the set number of the input vectors and the average relative errors of the estimate values obtained with our macro-model. Reference values for the circuit's power dissipation are obtained using time delays from the Synopsys PowerCompiler. It is evident from this table that the function is more accurate estimating the average power in some cases than others. The given input metrics values are more accurate for the specify range between [0.2, 0.8] and less accurate between [0, 0.2] and [0.8, 1]. One important source of error comes from do not consider on the macro-model, the power consumption of interconnects (buses) among different IP macro-blocks, and also other factors like glitch activities. For an individual IP block, we reported just 1-2% error in [29], [22], [23]. But for the entire IP-based system with interconnects the error increases 20-30%. This error can be reduced by different techniques that improves the data-path of interconnects among IP macro-blocks. In our experiments, the average error is 26.15%.

The results demonstrate that the transition density D_{in} is very effective to estimate power dissipation and relatively linear to the power measures . The correlation metrics S_{in} and T_{in} do not affect significantly the power dissipation and are less sensitive than the transition density .We have noticed that the number of inputs do not influence the output metrics for some IP macro blocks , whereas for some blocks are vice versa . Regression analysis is performed to fit the model's coefficients . Fig . 5, illustrates the correlation between the simulated power estimation and the estimated power values . For test IP system , we measured a quite good correlation coefficient that is around 96%.

Dotted circles in Fig. 6, indicates those spots where the error is much larger and convergence coefficient decreases,

Table 2. Accuracy of power estimation

Test IP System	Average Error
Set-1	35.00%
Set-2	24.71%
Set-3	40.22%
Set-4	73.46%
Set-5	4.42%
Set-6	59.19%
Set-7	46.81%
Set-8	82.43%
Set-9	17.08%
Set-10	22.16%
Set-11	33.20%
Set-12	79.77%
Set-13	89.95%
Set-14	22.96%
Set-15	13.45%
Set-16	22.01%
Set-17	86.28%
Set-18	3.00%
Set-19	39.65%
Set-20	19.18%
Set-21	35.09%
Set-22	60.56%
Set-23	66.49%
Set-24	63.01%
Set-25	38.37%

especially when the given input metrics values is between [0, 0.2] or [0.8, 1].

The minimum simulations length can be determined through convergence analysis. Converging on the average power figure help us to identify the minimum length necessary for each simulation, by considering when the power consumption gets close to a steady value. The sequences generated by our GA have high convergence and uniformity. Fig. 7. plots the variation of the power value with the trial interval

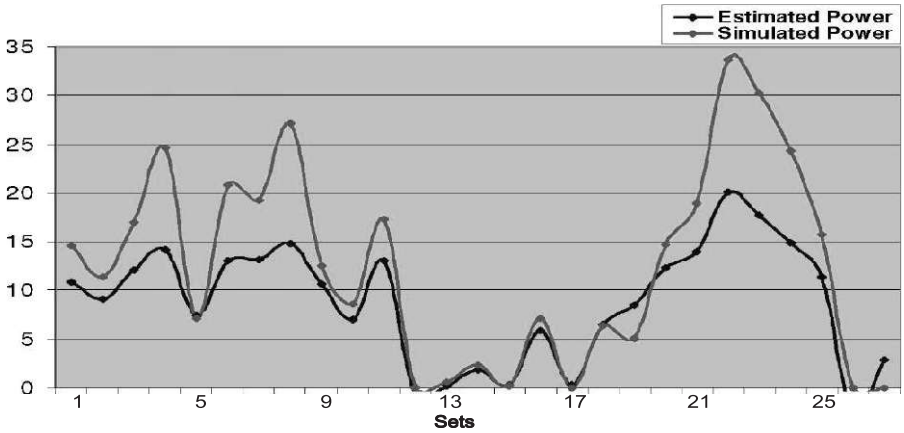

Fig .5 .Power comparison between macro model and reference simulated power

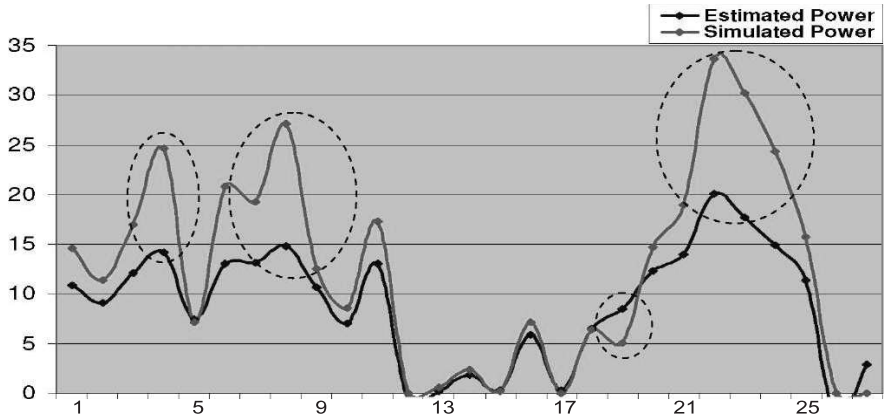

Fig .6 .Larger error spots for metric values between [0, 0.2] or [0.8, 1]

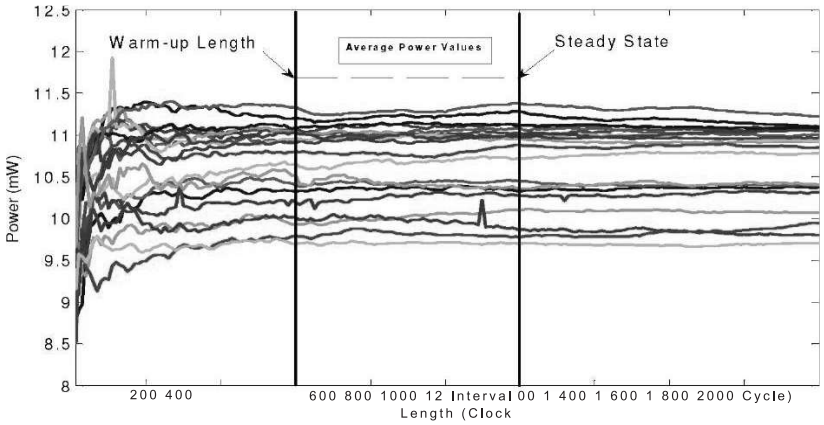

Fig .7 .Power changes with respect to sequence length for test IP based block

length. The figure shows that the interval length is 2000 for the IP system. The warm-up length is about 600 while the vertical line represents the steady state value at 1200.

5. Conclusion

A new power macro-modeling technique has been presented for high-level power estimation applied on a test IP-based system using different IP macro-blocks. In the preliminary work, for an individual IP blocks, we measured just 1-2% error. But for an entire IP-based system with interconnects between those blocks, the error is 20-30%. This is because the macro-model should consider the power consumption of interconnects among different IP macro-blocks and other factors like glitches. We demonstrated relatively better accuracy in some cases than in others. Our model showed an average error of 26.15% and a correlation coefficient of 96%. We found that considering output metrics in macro-model can only improves 2-5% accuracy. Currently, we are evaluating our macro-model on other test IP-based systems to improve its accuracy.

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